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09/653,272	08/31/2000	Salman Akram	4181US (96-973.2)	4727

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EXAMINER	
GARLAND, STEVEN R	
ART UNIT	PAPER NUMBER
2125	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/653,272	AKRAM ET AL.	
	Examiner	Art Unit	
	Steven R. Garland	2125	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *4/15/05,3/7/05*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,6-26,28-41,43,45-63 and 65-108* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-3,6-24,28-41,43,45-59 and 80-108* is/are allowed.

6)☒ Claim(s) *25,26,60-63 and 65-79* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *4/15/05,3/7/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

2. Claims 25 and 26 are rejected under 35 U.S.C. 102(e) as being anticipated by Beffa 5,915,231 (cited by applicant) .

Beffa discloses identification of an IC, use of a fuse or optical ID, reading the ID, storing data associated with the ID; testing, and accessing data to control processing. Beffa further teaches singulating; forming MCM devices, curing, bonding, sawing, etc. See the abstract; figures; col. 1, lines 28-67; col. 2, line 29 to col. 3, line 47; col. 3, line 59 to col. 4, line 44; and note the claims. Further note is taken that the devices when correctly processed have information associated with the ID that provides information as to the processes they have undergone.

In response to applicants' arguments, claims 25 and 26 are rejected under 35 U.S.C. 102(e) not (b). Further while common ownership might overcome a rejection under 35 U.S.C. 103, it does not overcome a rejection under 35 U.S.C. 102(e). Note MPEP 706.02(l)(3).

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 60-63,65-68,73, and 74 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beffa 5,915,231 (cited by applicant) in view of Moon et al. 5,326,709.

Beffa discloses identification of an IC, use of a fuse or optical ID, reading the ID, storing data associated with the ID; testing, and accessing data to control processing. Beffa further teaches singulating; forming MCM devices, curing, bonding, sawing, etc. See the abstract; figures; col. 1, lines 28-67; col. 2, line 29 to col. 3, line 47; col. 3, line 59 to col. 4, line 44; and note the claims. Further note is taken that the devices when correctly processed have information associated with the ID that provides information as to the processes they have undergone.

Beffa however does not teach the use of a dot or bar code, but does teach in col. 4, lines 20-25, the use of any type of code.

Moon et al. teaches the use of a dot code on dies. See col. 5, line 47 to col. 6, line 6.

It would have been obvious to one of ordinary skill in the art to modify Beffa in view of Moon and use a known dot or bar code to implement the code of Beffa for ease in implementing the code.

In response to applicant's arguments, the instant application is Continuation in Part of U.S. application 09/292,655 which is a continuation of U.S. application 08/871,015. However the "dot code" limitations now being claimed in instant claim 60 and its dependent claim only finds support in the instant application and were not disclosed in the parent applications. Thus the Beffa reference also qualifies as prior art under 35 U.S.C. 102(a,b) for the instant claim limitations.

6. Applicant has provided evidence in this file showing that the invention was owned by, or subject to an obligation of assignment to, the same entity as Beffa 5,915,231 at the time this invention was made, or was subject to a joint research agreement at the time this invention was made. However, reference Beffa 5,915,231 additionally qualifies as prior art under another subsection of 35 U.S.C. 102, and therefore, is not disqualified as prior art under 35 U.S.C. 103(c).

Applicant may overcome the applied art either by a showing under 37 CFR 1.132 that the invention disclosed therein was derived from the invention of this application,

and is therefore, not the invention "by another," or by antedating the applied art under 37 CFR 1.131.

7. Claims 69-72 and 75-79 are rejected under 35 U.S.C. 103(a) as being unpatentable over Beffa 5,915,231 in view of Moon et al. 5,326,709 as applied to claims 60-63,65-68,73, and 74 above, and further in view of Vu et al. 5,256,562 (cited by applicant).

Beffa discloses identification of an IC, use of a fuse or optical ID, reading the ID, storing data associated with the ID; testing, and accessing data to control processing. Beffa further teaches singulating; forming MCM devices, curing, bonding, sawing, etc. See the abstract; figures; col. 1, lines 28-67; col. 2, line 29 to col. 3, line 47; col. 3, line 59 to col. 4, line 44; and note the claims. Further note is taken that the devices when correctly processed have information associated with the ID that provides information as to the processes they have undergone.

Beffa however does not teach the use of a dot or bar code, but does teach in col. 4, lines 20-25, the use of any type of code.

. Moon et al. teaches the use of a dot code on dies. See col. 5, line 47 to col. 6, line 6.

It would have been obvious to one of ordinary skill in the art to modify Beffa in view of Moon and use a known dot or bar code to implement the code of Beffa for ease in implementing the code.

Beffa and Moon however do not teach the use of a laser or water jet for cutting. Beffa however does teach sawing and singulating. Note claim 23 of Beffa for example.

Vu et al. teaches the alternatives of a laser, water jet, or saw to separate semiconductor elements. See col. 7, lines 33-42.

It would have been obvious to one of ordinary skill in the art to modify Beffa and Moon in view of Vu and use a laser or water jet to separate (singulate) the devices. This would provide a longer lasting cutting element.

In response to applicant's arguments, the instant application is Continuation in Part of U.S. application 09/292,655 which is a continuation of U.S. application 08/871,015. However the "dot code" limitations now being claimed in instant claim 60 and its dependent claim only finds support in the instant application and were not disclosed in the parent applications. Thus the Beffa reference also qualifies as prior art under 35 U.S.C. 102(a,b) for the instant claim limitations. Also note paragraph 6 above.

8. Claims 1-3,6-24,28-41,43, 45-59, and 80-108 allowed.

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven R. Garland whose telephone number is 571-272-3741. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Leo Picard can be reached on 571-272-3749. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SRG

Steven R Garland
Examiner
Art Unit 2125

LEO PICARD
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

IN THE CLAIMS:

Claim 43 has been amended herein. All of the pending claims 1 through 3, 6 through 26, 28 through 41, 43, 45 through 63, and 65 through 108 are presented below. This listing of claims will replace all prior versions and listings of claims in the application. Please enter these claims as amended.

Please amend the claims as follows:

1. (Previously Presented) An integrated circuit manufacturing process using data related to manufacturing procedures used previously that a plurality of integrated circuits of Dynamic Random Access Memory (DRAM) semiconductor devices have undergone for selecting manufacturing procedures the plurality of integrated circuits of the Dynamic Random Access Memory (DRAM) semiconductor devices are to undergo, each Dynamic Random Access Memory (DRAM) semiconductor device having integrated circuits and having a substantially unique identification code, the manufacturing process comprising:

storing data in association with the identification code of each Dynamic Random Access Memory (DRAM) semiconductor device of the plurality identifying manufacturing procedures each Dynamic Random Access Memory (DRAM) semiconductor device has undergone, said storing data comprising storing data that identifies spare rows and columns used in repairing each DRAM semiconductor device;

automatically reading the identification code of each Dynamic Random Access Memory (DRAM) semiconductor device; and

accessing the data stored in association with the identification code of each Dynamic Random Access Memory (DRAM) semiconductor device.

2. (Original) The process of claim 1, further comprising:

selecting manufacturing procedures each semiconductor device undergoes in accordance with the accessed data.

3. (Previously Presented) The process of claim 1, wherein storing data comprises storing data that identifies repairs performed on each semiconductor device.

4. (Canceled)

5. (Canceled)

6. (Previously Presented) The process of claim 1, wherein storing data comprises storing data at probe.

7. (Previously Presented) The process of claim 1, wherein automatically reading the identification code of each semiconductor device comprises electrically retrieving a unique fuse ID programmed into each semiconductor device.

8. (Previously Presented) The process of claim 1, wherein automatically reading the identification code of each semiconductor device comprises optically reading a unique ID code provided on each semiconductor device.

9. (Previously Presented) The process of claim 8, wherein optically reading a unique ID code provided on each semiconductor device comprises optically reading a unique laser fuse ID programmed into each semiconductor device.

10. (Previously Presented) The process of claim 1, wherein automatically reading the identification code of each semiconductor device comprises automatically reading the identification code of each semiconductor device at one of an opens/shorts test, a burn-in test, and a back-end test in the integrated circuit manufacturing process.

11. (Previously Presented) The process of claim 1, wherein accessing the data stored in association with the identification code of each semiconductor device comprises accessing the data stored in association with the identification code of each semiconductor device at one of an opens/shorts test, a burn-in test, and a back-end test in the integrated circuit manufacturing process.

12. (Previously Presented) The process of claim 2, wherein selecting the manufacturing procedures each semiconductor device undergoes in accordance with the accessed data comprises selecting repairs each semiconductor device undergoes in accordance with the accessed data.

13. (Previously Presented) The process of claim 12, wherein each semiconductor device comprises Dynamic Random Access Memory (DRAM) semiconductor device, wherein selecting repairs each semiconductor device undergoes comprises selecting spare rows and columns used to repair each DRAM semiconductor device.

14. (Previously Presented) The process of claim 2, wherein selecting manufacturing procedures each semiconductor device undergoes in accordance with the accessed data comprises selecting whether each semiconductor device undergoes repair procedures.

15. (Previously Presented) The process of claim 14, wherein each semiconductor device comprises a Dynamic Random Access Memory (DRAM) semiconductor device, and wherein selecting whether each semiconductor device undergoes repair procedures comprises selecting whether each DRAM semiconductor device will be repaired in accordance with whether the accessed data indicates enough spare rows and columns are available in each semiconductor device to effect repairs.

16. (Previously Presented) The process of claim 2, wherein selecting manufacturing procedures each semiconductor device will undergo in accordance with the accessed data comprises determining whether each semiconductor device will be assembled into Multi-Chip Modules (MCM's) in accordance with whether the accessed data indicates each semiconductor device is repairable.

17. (Previously Presented) The process of claim 1, further comprising assembling each semiconductor device into a packaged semiconductor device after the step of storing data and before the step of automatically reading the identification code of each semiconductor device.

18. (Previously Presented) A method of manufacturing integrated circuit Dynamic Random Access Memory (DRAM) semiconductor devices from semiconductor wafers, the method comprising:

providing a plurality of semiconductor wafers;

fabricating a plurality of Dynamic Random Access Memory (DRAM) semiconductor devices on each of the wafers;

causing each Dynamic Random Access Memory (DRAM) semiconductor device of the plurality on each of the wafers to store a substantially unique identification code;

storing data in association with the identification code of each Dynamic Random Access Memory (DRAM) semiconductor device of the plurality that identifies manufacturing procedures each Dynamic Random Access Memory (DRAM) semiconductor device has undergone, said storing data comprising storing data that identifies spare rows and columns used in repairing each DRAM semiconductor device;

separating each Dynamic Random Access Memory (DRAM) semiconductor device of the plurality on each of the wafers from its wafer to form one Dynamic Random Access Memory (DRAM) semiconductor device of a plurality of Dynamic Random Access Memory (DRAM) semiconductor devices;

assembling each Dynamic Random Access Memory (DRAM) semiconductor device into a Dynamic Random Access Memory (DRAM) semiconductor device assembly;

automatically reading the identification code associated with each Dynamic Random Access Memory (DRAM) semiconductor device; and

accessing the data stored in association with the identification code associated with each Dynamic Random Access Memory (DRAM) semiconductor device.

19. (Previously Presented) The method of claim 18, further comprising:

selecting manufacturing procedures each semiconductor device undergoes in accordance with the accessed data.

20. (Previously Presented) The method of claim 18, wherein fabricating a plurality of semiconductor devices on each of the wafers comprises fabricating semiconductor devices selected from a group comprising Dynamic Random Access Memory (DRAM) semiconductor devices, Static Random Access Memory (SRAM) semiconductor devices, Synchronous DRAM (SDRAM) semiconductor devices, processor semiconductor devices, Rambus in-line memory module type semiconductor devices, small outline Rambus in-line memory module type semiconductor devices, and personal computer memory format type semiconductor devices.

21. (Previously Presented) The method of claim 18, wherein causing each semiconductor device on each of the wafers to store a substantially unique identification code comprises programming each semiconductor device on each of the wafers to permanently store a unique fuse ID.

22. (Previously Presented) The method of claim 21, wherein programming each semiconductor device on each of the wafers to permanently store a unique fuse ID comprises programming at least one of fuses and anti-fuses in each semiconductor device on each of the wafers to permanently store a unique fuse identification.

23. (Previously Presented) The method of claim 18, wherein assembling each semiconductor device of the semiconductor devices into a semiconductor device assembly comprises:

picking each semiconductor device from its wafer;

placing each semiconductor device onto an epoxy-coated bonding site of one lead frame of a plurality of lead frames;

curing the epoxy on the bonding site of each lead frame of the lead frames;

wire bonding each semiconductor device to its associated lead frame;

encapsulating each semiconductor device and its associated lead frame to form one of a plurality of semiconductor device assembly packages, each package having projecting leads;

curing each of the semiconductor device assembly packages;

de-flashing the projecting leads of each semiconductor device assembly package;

electroplating the projecting leads of each semiconductor device assembly package; and

singulating each semiconductor device assembly package into one semiconductor device assembly package of a plurality of discrete semiconductor device assembly packages.

24. (Previously Presented) The method of claim 18, wherein assembling each semiconductor device into a semiconductor device assembly comprises assembling each semiconductor device into a semiconductor device assembly selected from a group comprising a wire bond/lead frame semiconductor device, a Chip-On-Board (COB) semiconductor device, a flip-chip semiconductor device, and a Board-Over-Chip (BOC) semiconductor device.

25. (Previously Presented) A method of manufacturing Multi-Chip Modules (MCM's) from semiconductor wafers, the MCM's selected from a group of Single In-Line Memory Modules (SIMM's) and Dual In-line Memory Modules (DIMM's), Rambus In-Line Memory Modules (RIMM), Small Outline Rambus In-Line Memory Modules (SO-RIMM), Personal Computer Memory Format (PCMCIA), and Board-Over-Chip type substrates, the method comprising:

providing a plurality of semiconductor wafers;

fabricating a plurality of semiconductor devices on each of the wafers;

causing each semiconductor device of the semiconductor devices on each of the wafers to store a substantially unique identification code;

storing data in association with the identification code of each semiconductor device of the semiconductor devices that identifies manufacturing procedures each semiconductor device of the semiconductor devices has undergone;

separating each semiconductor device of the semiconductor devices on each wafer of the plurality of semiconductor wafers from its wafer to form one semiconductor device of a plurality of semiconductor devices;

assembling one or more of the semiconductor devices into each of a plurality of MCM's;

automatically reading the identification code of each semiconductor device of the semiconductor devices in each MCM of the plurality of MCM's; and

accessing the data stored in association with the identification code of each semiconductor device of the semiconductor devices in each MCM of the plurality of MCM's.

26. (Original) The method of claim 25, further comprising:

selecting manufacturing procedures the semiconductor devices will undergo in accordance with the accessed data.

27. (Canceled)

28. (Previously Presented) A method of manufacturing Dynamic Random Access Memory (DRAM) semiconductor devices from semiconductor wafers, the method comprising:

providing a plurality of semiconductor wafers;

fabricating a plurality of Dynamic Random Access Memory (DRAM) semiconductor devices on each of the wafers;

electronically probing each Dynamic Random Access Memory (DRAM) semiconductor device of the Dynamic Random Access Memory (DRAM) semiconductor devices on each wafer of the plurality of semiconductor wafers to identify good, bad and repairable semiconductor devices on each wafer of the plurality of semiconductor wafers;

repairing the repairable Dynamic Random Access Memory (DRAM) semiconductor devices;

programming each Dynamic Random Access Memory (DRAM) semiconductor device of the Dynamic Random Access Memory (DRAM) semiconductor devices on each wafer of the plurality of semiconductor wafers to store a unique fuse identification;

storing data in association with the fuse identification of each of the Dynamic Random Access Memory (DRAM) semiconductor devices identifying repairs performed on each Dynamic Random Access Memory (DRAM) semiconductor device of the Dynamic Random Access Memory (DRAM) semiconductor devices, said storing data comprising storing data that identifies spare rows and columns used in repairing each DRAM semiconductor device;

mounting each wafer of the plurality of semiconductor wafers on an adhesive film;

sawing each Dynamic Random Access Memory (DRAM) semiconductor device of the Dynamic Random Access Memory (DRAM) semiconductor devices on each wafer of the plurality of wafers from its wafer to form one of a plurality of discrete Dynamic Random Access Memory (DRAM) semiconductor devices;

automatically picking each Dynamic Random Access Memory (DRAM) semiconductor device of the Dynamic Random Access Memory (DRAM) semiconductor devices from its wafer;

placing each Dynamic Random Access Memory (DRAM) semiconductor device of the Dynamic Random Access Memory (DRAM) semiconductor devices onto an epoxy-coated bonding site of one lead frame of a plurality of lead frames;

curing the epoxy on the bonding site of each lead frame of the lead frames;

wire bonding each Dynamic Random Access Memory (DRAM) semiconductor device of the Dynamic Random Access Memory (DRAM) semiconductor devices to its associated lead frame;

encapsulating each Dynamic Random Access Memory (DRAM) semiconductor device of the Dynamic Random Access Memory (DRAM) semiconductor devices and its associated lead frame to form one of a plurality of Dynamic Random Access Memory (DRAM) semiconductor device assembly packages, each Dynamic Random Access Memory (DRAM) semiconductor device assembly package having projecting leads;

curing each Dynamic Random Access Memory (DRAM) semiconductor device assembly package;

de-flashing the projecting leads of each Dynamic Random Access Memory (DRAM) semiconductor device package;

electroplating the projecting leads of each Dynamic Random Access Memory (DRAM) semiconductor device package;

singulating each Dynamic Random Access Memory (DRAM) semiconductor device package;

testing each Dynamic Random Access Memory (DRAM) semiconductor device assembly package for opens and shorts;

burn-in testing each Dynamic Random Access Memory (DRAM) semiconductor device assembly package;

back-end testing each Dynamic Random Access Memory (DRAM) semiconductor device assembly package;

automatically reading an ID of each Dynamic Random Access Memory (DRAM) semiconductor device assembly package;

accessing data stored in association with the ID of each Dynamic Random Access Memory (DRAM) semiconductor device assembly package;

for any Dynamic Random Access Memory (DRAM) semiconductor device assembly package failing any one of the opens/shorts, burn-in, and back-end tests, evaluating the accessed data to determine whether the failing semiconductor device assembly package may be repaired;

repairing the Dynamic Random Access Memory (DRAM) semiconductor device assembly package determined in accordance with the accessed data to be repairable and returning the repaired Dynamic Random Access Memory (DRAM) semiconductor device assembly package to the semiconductor manufacturing process; and

discarding the Dynamic Random Access Memory (DRAM) semiconductor device assembly package determined in accordance with the accessed data to be unrepairable.

29. (Previously Presented) The method of claim 28, wherein mounting the wafers comprises mounting each wafer of the plurality of semiconductor wafers on an ultraviolet (U.V.) adhesive film, wherein the method further comprises exposing the U.V. adhesive film to U.V. light to loosen the wafers from the film prior to picking and placing each semiconductor device.

30. (Original) The method of claim 28, further comprising receiving a plurality of unrepairable semiconductor devices diverted from another semiconductor device manufacturing process.

31. (Previously Presented) A method of manufacturing Multi-Chip Modules (MCM's) from semiconductor wafers using Chip-On-Board (COB) techniques, the method comprising:

providing a plurality of semiconductor wafers;

fabricating a plurality of semiconductor devices on each wafer of the plurality of semiconductor wafers;

electronically probing each semiconductor device of the semiconductor devices on each wafer of the plurality of semiconductor wafers to identify good, bad and repairable semiconductor devices on each wafer of the plurality of semiconductor wafers;

repairing the repairable semiconductor devices;

programming each semiconductor device of the plurality of semiconductor devices on each wafer of the plurality of semiconductor wafers to store a unique fuse identification;

storing an electronic wafer map for each wafer of the plurality that identifies locations of good and bad semiconductor devices on each wafer and associates each semiconductor device on each wafer with its fuse identification;

storing data in association with the fuse identification of each semiconductor device of the semiconductor devices identifying repairs performed on each semiconductor device of the semiconductor devices;

mounting each wafer of the plurality of semiconductor wafers on an adhesive film;

sawing each semiconductor device of the semiconductor devices on each wafer of the plurality of semiconductor wafers from its wafer to form one discrete semiconductor device;

accessing the stored wafer map for each wafer of the plurality;

accessing the stored data for each semiconductor device on each wafer of the plurality of semiconductor wafers;

automatically picking each semiconductor device of the good semiconductor devices from its wafer;

discarding non-picked semiconductor devices identified as bad by the accessed wafer maps;

diverting picked semiconductor devices identified as good but unrepairable by the accessed wafer maps and data to a non-MCM semiconductor manufacturing process;

placing picked semiconductor devices identified as good and repairable by the accessed wafer maps and data onto epoxy-coated bonding sites of a plurality of printed circuit boards using COB techniques to form a plurality of MCM's;

curing the epoxy on the bonding sites of each MCM of the plurality of MCM's;

wire bonding each of the semiconductor devices to its associated MCM;

testing each semiconductor device of the semiconductor devices on each MCM of the plurality of MCM's for opens and shorts;

encapsulating each semiconductor device of the semiconductor devices on each MCM of the plurality of MCM's;

retesting each semiconductor device of the semiconductor devices on each MCM of the plurality of MCM's for opens and shorts;

burn-in testing each semiconductor device of the semiconductor devices on each MCM of the plurality of MCM's;

back-end testing each semiconductor device of the semiconductor devices on each MCM of the plurality of MCM's;

automatically reading the fuse identification of each semiconductor device in each MCM of the plurality of MCM's;

accessing the data stored in association with the fuse identification of each semiconductor device of the semiconductor devices;

for any semiconductor device of the semiconductor devices failing any one of the opens/shorts, burn-in, and back-end tests, evaluating the accessed data to determine whether the failing semiconductor device may be repaired;

repairing any semiconductor device of the semiconductor devices determined in accordance with the accessed data to be repairable and returning repaired MCM's to the manufacturing process; and

replacing any semiconductor device of the semiconductor devices determined in accordance with the accessed data to be unrepairable with a Known Good Die (KGD) and returning the repaired MCM's to the manufacturing process.

32. (Previously Presented) The method of claim 31, further comprising plasma cleaning each MCM of the plurality of MCM's after curing the epoxy on the bonding sites of each MCM.

33. (Previously Presented) The method of claim 31, wherein mounting the wafers comprises mounting each wafer of the plurality of semiconductor wafers on an Ultraviolet (U.V.) adhesive film, wherein the method further comprises exposing the U.V. adhesive film to U.V. light to loosen the wafer from the film prior to picking and placing each semiconductor device.

34. (Original) The method of claim 31, further comprising singulating the printed circuit boards associated with each MCM of the plurality of MCM's.

35. (Previously Presented) A method of manufacturing Multi-Chip Modules (MCM's) from semiconductor wafers using flip-chip techniques, the method comprising:

providing a plurality of semiconductor wafers;

fabricating a plurality of semiconductor devices on each wafer of the semiconductor wafers;

electronically probing each semiconductor device of the semiconductor devices on each wafer of the plurality of wafers to identify good, bad and repairable semiconductor devices on each wafer of the plurality of wafers;

repairing the repairable semiconductor devices;

programming each semiconductor device of the semiconductor devices on each wafer of the plurality of wafers to store a unique fuse identification;

storing an electronic wafer map for each wafer of the plurality that identifies locations of good and bad semiconductor devices on each wafer and associates each semiconductor device on each wafer with its fuse identification;

storing data in association with the fuse identification of each semiconductor device of the semiconductor devices identifying repairs performed on each semiconductor device of the semiconductor devices;

mounting each wafer of the plurality of wafers on an adhesive film;

sawing each semiconductor device of the semiconductor devices on each wafer of the wafers from its wafer to form a semiconductor device;

accessing the stored wafer map for each wafer of the plurality;

accessing the stored data for each semiconductor device of the semiconductor devices on each of the wafers;

automatically picking each semiconductor device of the good semiconductor devices from its wafer;

discarding non-picked semiconductor devices identified as bad by the accessed wafer maps;

diverting picked semiconductor devices identified as good but unrepairable by the accessed wafer maps and data to a non-MCM device manufacturing process;

flip-chip attaching picked semiconductor devices identified as good and repairable by the accessed wafer maps and data to bonding sites of each printed circuit board of a plurality of printed circuit boards to form a plurality of MCM's;

curing each MCM of the plurality of MCM's;

testing each semiconductor device of the semiconductor devices on each MCM of the plurality of MCM's for opens and shorts;

encapsulating each semiconductor device of the semiconductor devices on each MCM of the plurality of MCM's;

retesting each semiconductor device of the semiconductor devices on each MCM of the plurality of MCM's for opens and shorts;

burn-in testing each semiconductor device of the semiconductor devices on each MCM of the plurality MCM's;

back-end testing each semiconductor device of the semiconductor devices on each MCM of the plurality of MCM's;

automatically reading the fuse identification of each semiconductor device of the semiconductor devices in each MCM of the plurality of MCM's;

accessing the data stored in association with the fuse identification of each semiconductor device of the semiconductor devices in each MCM of the plurality of MCM's;

for any semiconductor device of the semiconductor devices on each MCM of the plurality failing any one of the opens/shorts, burn-in, and back-end tests, evaluating the accessed data to determine whether the failing semiconductor devices may be repaired;

repairing any semiconductor device of the semiconductor devices determined in accordance with the accessed data to be repairable and returning repaired MCM's to the manufacturing process; and

replacing any semiconductor device of the semiconductor devices determined in accordance with the accessed data to be unrepairable with a Known Good Die (KGD) and returning the repaired MCM's to the manufacturing process.

36. (Previously Presented) The method of claim 35, wherein mounting the wafers comprises mounting each wafer of the plurality of wafers on an Ultraviolet (U.V.) adhesive film, wherein the method further comprises exposing the U.V. adhesive film to U.V. light to loosen the wafer from the film prior to picking and flip-chip attaching each semiconductor device.

37. (Original) The method of claim 35, further comprising singulating the printed circuit boards associated with each MCM of the plurality of MCM's.

38. (Previously Presented) A method in an integrated circuit semiconductor device in a Multi-Chip Module (MCM) manufacturing process for diverting good but unrepairable semiconductor devices from the process, the semiconductor devices being of the type to have a substantially unique identification code, the method comprising:

storing data in association with the identification code of each semiconductor device of the semiconductor devices identifying semiconductor devices that are good and repairable, that are good but unrepairable, and that are bad;

automatically reading the identification code of each semiconductor device of the semiconductor devices;

accessing the data stored in association with the identification code of each semiconductor device of the semiconductor devices;

diverting semiconductor devices identified as good but unrepairable by the accessed data to one of use in other semiconductor device manufacturing processes and discarding the semiconductor devices identified as good but unrepairable; and

discarding semiconductor devices identified as bad by the accessed data.

39. (Original) The method of claim 38, further comprising:

assembling at least one semiconductor device identified as good and repairable into at least one MCM.

40. (Previously Presented) A semiconductor device manufacturing process using data related to manufacturing procedures used previously that a plurality of integrated circuits of semiconductor devices have undergone for selecting manufacturing procedures the plurality of integrated circuits of the semiconductor devices are to undergo during manufacture, each semiconductor device having integrated circuits and having a substantially unique identification code, the manufacturing process comprising:

storing data in association with the identification code of each semiconductor device of the semiconductor devices identifying manufacturing procedures the semiconductor device has undergone, said storing data comprising storing data that identifies repairs performed on each semiconductor device;

automatically reading the identification code of each semiconductor device; and

accessing the data stored in association with the identification code of each semiconductor device.

41. (Original) The process of claim 40, further comprising:

selecting manufacturing procedures each semiconductor device undergoes in accordance with the accessed data.

42. (Canceled)

43. (Currently Amended) The process of claim 40 ~~42~~, wherein each semiconductor device comprises Dynamic Random Access Memory (DRAM) semiconductor device, wherein storing data comprises storing data that identifies spare rows and columns used in repairing each DRAM semiconductor device.

44. (Canceled)

45. (Previously Presented) The process of claim 40, wherein storing data comprises storing data at probe.

46. (Previously Presented) The process of claim 40, wherein automatically reading the identification code of each semiconductor device comprises electrically retrieving a unique fuse ID programmed into each semiconductor device.

47. (Previously Presented) The process of claim 40, wherein the identification code of each semiconductor device comprises an identification code including one of a fuse ID, dot code, and bar code.

48. (Previously Presented) The process of claim 40, wherein the identification code of each semiconductor device comprises a dot code.

49. (Previously Presented) The process of claim 40, wherein the identification code of each semiconductor device comprises an identification code including a bar code.

50. (Previously Presented) The process of claim 40, wherein automatically reading the identification code of each semiconductor device comprises optically reading a unique ID code provided on each semiconductor device.

51. (Previously Presented) The process of claim 50, wherein optically reading a unique ID code provided on each semiconductor device comprises optically reading a unique laser fuse ID programmed into each semiconductor device.

52. (Previously Presented) The process of claim 40, wherein automatically reading the identification code of each semiconductor device comprises automatically reading the identification code of each semiconductor device at one of an opens/shorts test, a burn-in test, and a back-end test in the semiconductor device manufacturing process.

53. (Previously Presented) The process of claim 40, wherein accessing the data stored in association with the identification code of each semiconductor device comprises accessing the data stored in association with the identification code of each semiconductor device at one of an opens/shorts test, a burn-in test, and a back-end test in the semiconductor device manufacturing process.

54. (Previously Presented) The process of claim 41, wherein selecting the manufacturing procedures each semiconductor device undergoes in accordance with the accessed data comprises selecting repairs each semiconductor device undergoes in accordance with the accessed data.

55. (Previously Presented) The process of claim 54, wherein each semiconductor device comprises a Dynamic Random Access Memory (DRAM) semiconductor device, and wherein selecting repairs each semiconductor device undergoes comprises selecting spare rows and columns used to repair the DRAM semiconductor device.

56. (Previously Presented) The process of claim 41, wherein selecting manufacturing procedures each semiconductor device undergoes in accordance with the accessed data comprises selecting whether each semiconductor device undergoes repair procedures.

57. (Previously Presented) The process of claim 56, wherein each semiconductor device comprises a Dynamic Random Access Memory (DRAM) semiconductor device, and wherein selecting whether each semiconductor device undergoes repair procedures comprises selecting whether each DRAM semiconductor device will be repaired in accordance with whether the accessed data indicates enough spare rows and columns are available in each semiconductor device to effect repairs.

58. (Previously Presented) The process of claim 41, wherein selecting manufacturing procedures each semiconductor device will undergo in accordance with the accessed data comprises determining whether each semiconductor device will be assembled into Multi-Chip Modules (MCM's) in accordance with whether the accessed data indicates each semiconductor device is repairable.

59. (Previously Presented) The process of claim 40, further comprising assembling each semiconductor device into a packaged semiconductor device after the step of storing data and before the step of automatically reading the identification code of each semiconductor device.

60. (Previously Presented) A method of manufacturing semiconductor devices from wafers, the method comprising:

providing a plurality of wafers;

fabricating a plurality of semiconductor devices on at least one wafer of the plurality of wafers;

causing each semiconductor device of the plurality on the at least one wafer to store a substantially unique identification code, said causing each of the semiconductor devices to store a substantially unique identification code comprising applying a dot code to each of the semiconductor devices;

storing data in association with the identification code of each semiconductor device that identifies manufacturing procedures each semiconductor device has undergone;

separating each semiconductor device on the at least one wafer from the at least one wafer to form at least one semiconductor device;

assembling the at least one semiconductor device into a semiconductor device assembly;

automatically reading the identification code associated with the at least one semiconductor device; and

accessing the data stored in association with the identification code associated with the at least one semiconductor device.

61. (Original) The method of claim 60, further comprising:

selecting manufacturing procedures the at least one semiconductor device undergoes in accordance with the accessed data.

62. (Previously Presented) The method of claim 60, wherein fabricating a plurality of semiconductor devices on at least one wafer comprises fabricating semiconductor devices selected from a group comprising Dynamic Random Access Memory (DRAM) semiconductor devices, Static Random Access Memory (SRAM) semiconductor devices, Synchronous DRAM (SDRAM) semiconductor devices, processor semiconductor devices, Rambus in-line memory module type semiconductor devices, small outline Rambus in-line memory module type semiconductor devices, and personal computer memory format type semiconductor devices.

63. (Previously Presented) The method of claim 60, wherein causing each of the semiconductor devices to store a substantially unique identification code comprises programming each semiconductor device on the at least one wafer to permanently store a unique fuse ID.

64. (Canceled)

65. (Previously Presented) The method of claim 60, wherein causing each of the semiconductor devices to store a substantially unique identification code comprises applying a bar code to each of the semiconductor devices.

66. (Previously Presented) The method of claim 63, wherein programming each semiconductor device on the at least one wafer to permanently store a unique fuse ID code comprises programming at least one of fuses and anti-fuses in each semiconductor device on the at least one wafer to permanently store the unique fuse ID.

67. (Previously Presented) The method of claim 60, wherein assembling the at least one semiconductor device into a semiconductor device assembly comprises:

picking each of the plurality of semiconductor devices from the at least one wafer;

placing each semiconductor device onto an epoxy-coated bonding site of one lead frame of a plurality of lead frames;

curing the epoxy on the bonding site of each lead frame of the lead frames;

wire bonding each semiconductor device to its associated lead frame;

encapsulating each semiconductor device and its associated lead frame to form one of a plurality of semiconductor device assembly packages, each package having projecting leads;

curing each of the semiconductor device assembly packages;

de-flashing the projecting leads of each semiconductor device assembly package;

electroplating the projecting leads of each semiconductor device assembly package; and

singulating each semiconductor device assembly package into one semiconductor device assembly package of a plurality of discrete semiconductor device assembly packages.

68. (Previously Presented) The method of claim 60, wherein separating each semiconductor device on the at least one wafer from the at least one wafer to form at least one semiconductor device and wherein the step of assembling the at least one semiconductor device into a semiconductor device assembly comprise:

singulating at least one semiconductor device of the plurality from the at least one wafer using a saw.

69. (Previously Presented) The method of claim 60, wherein separating each semiconductor device on the at least one wafer from the at least one wafer to form at least one semiconductor device and wherein the step of assembling the at least one semiconductor device into a semiconductor device assembly comprise:

singulating at least one semiconductor device of the plurality from the at least one wafer using a laser.

70. (Previously Presented) The method of claim 60, wherein separating each semiconductor device on the at least one wafer from the at least one wafer to form at least one semiconductor device and wherein the step of assembling the at least one semiconductor device into a semiconductor device assembly comprises:

singulating at least one semiconductor device of the plurality from the at least one wafer using a laser/water apparatus.

71. (Previously Presented) The method of claim 60, wherein separating each semiconductor device on the at least one wafer from the at least one wafer to form at least one semiconductor device and wherein the step of assembling the at least one semiconductor device into a semiconductor device assembly comprises:

singulating at least one semiconductor device of the plurality from the at least one wafer using a cool laser apparatus.

72. (Previously Presented) The method of claim 60, wherein separating each semiconductor device on the at least one wafer from the at least one wafer to form at least one semiconductor device and wherein the step of assembling the at least one semiconductor device into a semiconductor device assembly comprises:

singulating at least one semiconductor device of the plurality from the at least one wafer using a water jet apparatus.

73. (Previously Presented) The method of claim 60, wherein assembling the at least one semiconductor device into a semiconductor device assembly comprises assembling the at least one semiconductor device into a semiconductor device assembly selected from a group comprising a wire bond/lead frame semiconductor device, a Chip-On-Board (COB) semiconductor device, a flip-chip semiconductor device, and a Board-Over-Chip (BOC) semiconductor device.

74. (Previously Presented) The method of claim 60, wherein assembling the at least one semiconductor device into a semiconductor device assembly comprises:

mounting the at least one semiconductor device on one of a lead frame of a plurality of lead frames and a substrate;

encapsulating the at least one semiconductor device and a portion of the one of a lead frame and a substrate, forming a semiconductor device assembly package; and

singulating the semiconductor device assembly package from the one of a plurality of lead frames and a substrate to form one semiconductor device assembly package.

75. (Previously Presented) The method of claim 74, wherein singulating the semiconductor device assembly package from the one of a plurality of lead frames and a substrate to form one semiconductor device assembly package comprises the use of a saw.

76. (Previously Presented) The method of claim 74, wherein singulating the semiconductor device assembly package from the one of a plurality of lead frames and a substrate to form one semiconductor device assembly package comprises the use of a laser.

77. (Previously Presented) The method of claim 74, wherein singulating the semiconductor device assembly package from the one of a plurality of lead frames and a substrate to form one semiconductor device assembly package comprises the use of a laser/water apparatus.

78. (Previously Presented) The method of claim 74, wherein singulating the semiconductor device assembly package from the one of a plurality of lead frames and a substrate to form one semiconductor device assembly package comprises the use of a cool laser.

79. (Previously Presented) The method of claim 74, wherein singulating the semiconductor device assembly package from the one of a plurality of lead frames and a substrate to form one semiconductor device assembly package comprises the use of a water jet.

80. (Previously Presented) A method of manufacturing semiconductor devices from a plurality of wafers, the method comprising:

providing a plurality of wafers;

fabricating a plurality of semiconductor devices on at least one wafer of the plurality of wafers;

causing at least one semiconductor device of the plurality on the at least one wafer to store a substantially unique identification code;

storing data in association with the identification code of the at least one semiconductor device identifying manufacturing procedures the at least one semiconductor device has undergone, said storing data comprising storing data that identifies repairs performed on each semiconductor device;

separating the at least one semiconductor device and at least one other semiconductor device on the at least one wafer from the at least one wafer to form at least two semiconductor devices on a portion of the at least one wafer;

assembling the at least two semiconductor devices into a semiconductor device assembly;

automatically reading the identification code associated with the at least two semiconductor devices; and

accessing the data stored in association with the identification code associated with the at least two semiconductor devices.

81. (Original) The method of claim 80, further comprising:

selecting manufacturing procedures the at least one semiconductor device undergoes in accordance with the accessed data.

82. (Previously Presented) The method of claim 80, wherein fabricating a plurality of semiconductor devices on at least one wafer comprises fabricating semiconductor devices selected from a group comprising Dynamic Random Access Memory (DRAM) semiconductor devices, Static Random Access Memory (SRAM) semiconductor devices, Synchronous DRAM (SDRAM) semiconductor devices, processor semiconductor devices, Rambus in-line memory module type semiconductor devices, small outline Rambus in-line memory module type semiconductor devices, and personal computer memory format type semiconductor devices.

83. (Previously Presented) The method of claim 80, wherein causing the at least one semiconductor device to store a substantially unique identification code comprises programming the at least one semiconductor device on the at least one wafer to permanently store a unique fuse ID.

84. (Previously Presented) The method of claim 80, wherein causing the at least one semiconductor device to store a substantially unique identification code comprises applying a dot code to the at least one semiconductor device.

85. (Previously Presented) The method of claim 80, wherein causing the at least one semiconductor device to store a substantially unique identification code comprises applying a bar code to the at least one semiconductor device.

86. (Previously Presented) The method of claim 83, wherein programming the at least one semiconductor device on the at least one wafer to permanently store a unique fuse ID code comprises programming at least one of fuses and anti-fuses in the at least one semiconductor device on the at least one wafer to permanently store the unique fuse ID.

87. (Previously Presented) The method of claim 80, wherein assembling the at least two semiconductor devices into a semiconductor device assembly comprises:
picking the at least two semiconductor devices from the at least one wafer;

placing the at least two semiconductor devices onto a bonding site of a substrate;

encapsulating at least one semiconductor device of the at least two semiconductor devices to form one of at least one semiconductor device assembly package; and

singulating the at least one semiconductor device assembly package.

88. (Previously Presented) The method of claim 80, wherein separating the at least one semiconductor device and the at least one other semiconductor device on the at least one wafer from the at least one wafer to form at least two semiconductor devices on a portion of the at least one wafer comprises:

singulating the at least two semiconductor devices from the at least one wafer using a saw.

89. (Previously Presented) The method of claim 80, wherein separating the at least one semiconductor device and the at least one other semiconductor device on the at least one wafer from the at least one wafer to form at least two semiconductor devices on a portion of the at least one wafer comprises:

singulating the at least two semiconductor devices from the at least one wafer using a laser.

90. (Previously Presented) The method of claim 80, wherein separating the at least one semiconductor device and the at least one other semiconductor device on the at least one wafer from the at least one wafer to form at least two semiconductor devices on a portion of the at least one wafer comprises:

singulating the at least two semiconductor devices from the at least one wafer using a laser/water apparatus.

91. (Previously Presented) The method of claim 80, wherein separating the at least one semiconductor device and the at least one other semiconductor device on the at least one wafer from the at least one wafer to form at least two semiconductor devices on a portion of the at least one wafer comprises:

singulating the at least two semiconductor devices from the at least one wafer using a cool laser apparatus.

92. (Previously Presented) The method of claim 80, wherein separating the at least one semiconductor device and the at least one other semiconductor device on the at least one wafer from the at least one wafer to form at least two semiconductor devices on a portion of the at least one wafer comprises:

singulating the at least two semiconductor devices from the at least one wafer using a water jet apparatus.

93. (Previously Presented) The method of claim 80, wherein assembling the at least two semiconductor devices into a semiconductor device assembly comprises assembling the at least two semiconductor devices into a semiconductor device assembly selected from a group comprising a wire bond/lead frame semiconductor device, a Chip-On-Board (COB) semiconductor device, a flip-chip semiconductor device, and a Board-Over-Chip (BOC) semiconductor device.

94. (Original) The method of claim 80, wherein assembling the at least two semiconductor devices into a semiconductor device assembly comprises:

mounting the at least two semiconductor devices on a substrate;

encapsulating each semiconductor device and a portion of the substrate forming semiconductor device assembly packages; and

singulating the semiconductor device assembly packages.

95. (Previously Presented) The method of claim 94, wherein singulating the semiconductor device assembly package comprises the use of a saw.

96. (Previously Presented) The method of claim 94, wherein singulating the semiconductor device assembly package comprises the use of a laser.

97. (Previously Presented) The method of claim 94, wherein singulating the semiconductor device assembly package comprises the use of a laser/water apparatus.

98. (Previously Presented) The method of claim 94, wherein singulating the semiconductor device assembly package comprises the use of a cool laser.

99. (Previously Presented) The method of claim 94, wherein singulating the semiconductor device assembly package comprises the use of a water jet.

100. (Previously Presented) A method of manufacturing semiconductor devices from a plurality of wafers, the method comprising:

providing a plurality of wafers;

fabricating a plurality of semiconductor devices on at least one wafer of the plurality of wafers;

causing at least one semiconductor device of the plurality on the at least one wafer to store a substantially unique identification code;

storing data in association with the identification code of the at least one semiconductor device identifying manufacturing procedures the at least one semiconductor device has undergone, said storing data comprising storing data that identifies repairs performed on each semiconductor device;

assembling the at least one wafer into a semiconductor device assembly;

automatically reading the identification code associated with the at least one semiconductor device; and

accessing the data stored in association with the identification code associated with the at least one semiconductor device.

101. (Original) The method of claim 100, further comprising:

selecting manufacturing procedures the at least one semiconductor device undergoes in accordance with the accessed data.

102. (Previously Presented) The method of claim 100, wherein fabricating a plurality of semiconductor devices on at least one wafer comprises fabricating semiconductor devices selected from a group comprising Dynamic Random Access Memory (DRAM) semiconductor devices, Static Random Access Memory (SRAM) semiconductor devices, Synchronous DRAM (SDRAM) semiconductor devices, processor semiconductor devices, Rambus in-line memory module type semiconductor devices, small outline Rambus in-line memory module type semiconductor devices, and personal computer memory format type semiconductor devices.

103. (Previously Presented) The method of claim 100, wherein causing the at least one semiconductor device to store a substantially unique identification code comprises programming the at least one semiconductor device on the at least one wafer to permanently store a unique fuse ID.

104. (Previously Presented) The method of claim 100, wherein causing the at least one semiconductor device to store a substantially unique identification code comprises applying a dot code to the at least one semiconductor device.

105. (Previously Presented) The method of claim 100, wherein causing the at least one semiconductor device to store a substantially unique identification code comprises applying a bar code to the at least one semiconductor device.

106. (Previously Presented) The method of claim 103, wherein programming the at least one semiconductor device on the at least one wafer to permanently store a unique fuse ID comprises programming at least one of fuses and anti-fuses in the at least one semiconductor device on the at least one wafer to permanently store the unique fuse ID.

107. (Previously Presented) The method of claim 100, wherein assembling the at least one wafer into a semiconductor device assembly comprises assembling the wafer into a semiconductor device assembly selected from a group comprising a Chip-On-Board (COB) semiconductor device, a flip-chip semiconductor device, and a Board-Over-Chip (BOC) semiconductor device.

108. (Previously Presented) The method of claim 100, wherein assembling the at least one wafer into a semiconductor device assembly comprises:

mounting the at least one wafer on a substrate; and

encapsulating the at least one wafer and a portion of the substrate, forming a wafer scale semiconductor device assembly package.